

META: Memory Exploration Tool for Android Devices

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Introduction and Motivation

- More than 2 billion mobile devices are being used today.^[1]
- With every passing year, new Android OS versions are being released and the diversity of applications supported is growing.
- With the rapid increase in usage of mobile devices, focus is needed on architecture of handheld devices to keep the mobile computing ecosystem evolving and in pace with people's expectations.
- DRAM being the primary contributor to SoC energy consumption^[2], increase it memory requirements will significantly increase power budget of SoC.

Tracer Module

• To enable the tracing functionality in Android Emulator, we modified the source code of translation path of QEMU.



Background

- Today, only 1 percent of all architecture research papers published each year in the top computer architecture conferences focus on mobile computing.^[1]
- We believe that this dearth of research is due to unavailability of tools supporting latest operating system platforms for the architectural studies of mobiles.
- The tools currently present GemDroid^[3], MofySim^[4] support only the older Android OS version (KitKat 4.4)
- Older versions of OS => older versions of apps which are not representative of the future apps.
- Simulators which allow user interaction are required as mobile apps involve significant amount of user interaction.

Original Translation Path print insn() Prints the instruction I the trace file target_disas() issasembles the que Instruction TCG Ops Guest tcg_gen_code() Is cached? gen intermediate code(Cache the translation Instructions epresentation om the cached transla **Modified Translation Path**

Contributions of META

META aims to catalyse research in field of mobile computer architecture by acting as a simulation tool which:

- Is compatible with all Android OS versions current and upcoming
- Allows accounting of effects of user interactions with devices during simulation
- Can perform comprehensive analysis of memory subsystem.

Memory Simulation Module

- Memory traces are generated from the raw instruction traces using a preprocessing module.
- The cache module simulates the behaviour of a N-level cache using the memory traces. It provides:
 - Cache statistics like hit rate, total requests etc.
 - Trace file containing memory traces for the main memory.

"level" : 1, "size" : 32768, "associativity" : 8, "sets" : 64, "read time" : 1, "write time" : 2

"level" : 2,



Tracer Module

Tool Diagram

META Tool Design

- META is built on top of the Android Emulator, shipped with the Android Open Source Project (AOSP)^[6].
- Android emulator uses Android Virtual Device(AVD) to specify hardware profile, system image, storage areas etc. of the device being simulated.
- For future compatibility, newer AVDs will have to be provided, which are typically shipped with AOSP, making the integration of future Android versions much smoother.

• The newly generated traces are fed to NVMain which return main memory statistics like bank power, refresh power, number of activates, precharges etc at a bank level.

channel0.rank0.bank1.bankEnergy 165824mA*t
channel0.rank0.bank1.activeEnergy 81459mA*t channel0.rank0.bank1.burstEnergy 35145mA*t channel0.rank0.bank1.refreshEnergy 49220mA*t channel0.rank0.bank1.bankPower 0.00409577W channel0.rank0.bank1.activePower 0.002012W channel0.rank0.bank1.burstPower 0.00 channel0.rank0.bank1.refreshPower 0.00121571W channel0.rank0.bank1.bandwidth 3239.79MB/s channel0.rank0.bank1.dataCycles 2308 channel0.rank0.bank1.powerCycles 60730 channel0.rank0.bank1.utilization 0.0380043 channel0.rank0.bank1.reads 367 channel0.rank0.bank1.writes 210 channel0.rank0.bank1.activates 431 channel0.rank0.bank1.precharges 430 channel0.rank0.bank1.refreshes 23 channel0.rank0.bank1.activeCycles 51643 channel0.rank0.bank1.standbyCycles 9087 channel0.rank0.bank1.fastExitActiveCycles 0
channel0.rank0.bank1.fastExitPrechargeCycles channel0.rank0.bank1.slowExitPrechargeCycles 0 channel0.rank0.bank1.actWaits 0 channel0.rank0.bank1.actWaitTotal 0 channel0.rank0.bank1.actWaitAverage -nar channel0.rank0.bank1.averageEndurance 0 channel0.rank0.bank1.worstCaseEndurance 18446744073709551615

Cache Hit rate



Output from NVMain

Potential Usecases

- Trace Generation
 - The traces can also be used to analyze instruction distribution profile.
- Cache Hierarchy Modeling
 - A custom N-level cache hierarchy can be modelled. Size, associativity and

"associativity" : 4, "sets" : 1024, "read time" : 10, "write time" : 15

"size" : 262144,

Cache configuration

- META has a modular design which enables outputs of multiple stages to be used independent of each other.
- The tool mainly consists of two modules:
 - Tracer Module
 - Memory Simulation Module.

- number of sets can be specified in the configuration file.
- DRAM, Non-volatile and Hybrid Memory Simulation
 - This can be done by altering the configuration files of NVMain. Configuration
 - files of PCM, STTRAM, RRAM and hybrid memory are shipped along with NVMain.

Future Plan

The tool has reached the final stages of development. After completing the development stage we plan to perform extensive testing of the tool to uncover all the corner cases. We intend to open source the tool once the testing stage is completed.

We also aim to create a benchmark of applications and simulate them using META to showcase the analysis that can be performed using META.

References

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